LM25574 42-V, 0.5-A Step-Down Switching Regulator

1 Features

- Integrated 42-V, 750-mΩ N-Channel MOSFET
- Ultra-Wide Input Voltage From 6 V to 42 V
- Adjustable Output Voltage as Low as 1.225 V
- 1.5% Feedback Reference Accuracy
- Operating Frequency Adjustable Between 50 kHz and 1 MHz With Single Resistor
- Master or Slave Frequency Synchronization
- Adjustable Soft-Start
- Emulated Current Mode Control Architecture
- Wide Bandwidth Error Amplifier
- Built-In Protection
- TSSOP-16 Package
- Create a Custom Design Using the LM25574 With the WEBENCH® Power Designer

2 Applications

- Industrial

3 Description

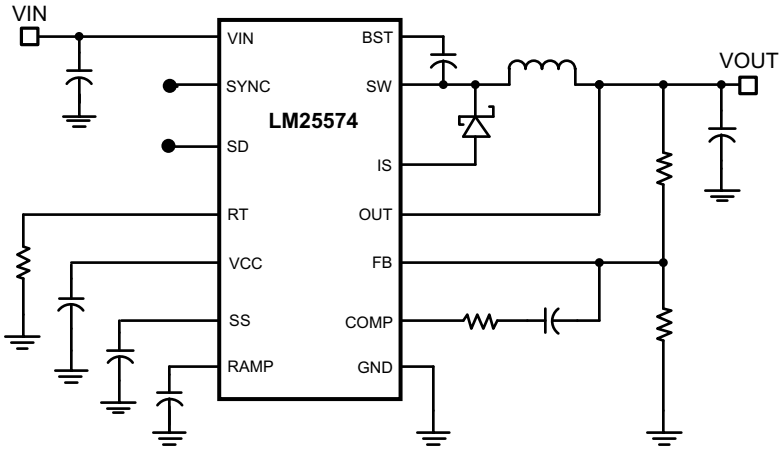
The LM25574 is an easy to use buck regulator which allows design engineers to design and optimize a robust power supply using a minimum set of components. Operating with an input voltage range of 6 V to 42 V, the LM25574 delivers 0.5-A of continuous output current with an integrated 750-mΩ N-Channel MOSFET. The regulator utilizes an Emulated Current Mode architecture which provides inherent line regulation, tight load transient response, and ease of loop compensation without the usual limitation of low-duty cycles associated with current mode regulators. The operating frequency is adjustable from 50 kHz to 1-MHz to allow optimization of size and efficiency. To reduce EMI, a frequency synchronization pin allows multiple IC's from the LM(2)557x family to self-synchronize or to synchronize to an external clock. The LM25574 guarantees robustness with cycle-by-cycle current limit, short-circuit protection, thermal shut-down, and remote shut-down. The device is available in a TSSOP-16 package. The LM25574 is supported by the full suite of WEBENCH® On-Line design tools.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM25574	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H	Page
• Added *Application and Implementation* section *Device Information* table, *Pin Configuration* and *Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision F (January 2007) to Revision G	Page
• Changed layout of National Data Sheet to TI format	23

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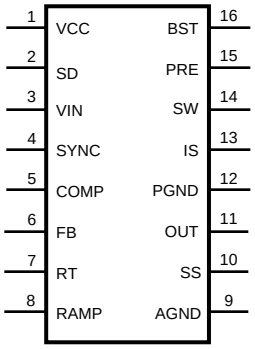
5 Pin Configuration and Functions

PW
16-Pin TSSOP
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	VCC	Output of the bias regulator Vcc tracks Vin up to 9 V. Beyond 9 V, Vcc is regulated to 7 Volts. A 0.1 uF to 1 uF ceramic decoupling capacitor is required. An external voltage (7.5 V – 14 V) can be applied to this pin to reduce internal power dissipation.
2	SD	Shutdown or UVLO input If the SD pin voltage is below 0.7 V the regulator will be in a low power state. If the SD pin voltage is between 0.7 V and 1.225 V the regulator will be in standby mode. If the SD pin voltage is above 1.225 V the regulator will be operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5 µA pull-up current source configures the regulator fully operational.
3	VIN	Input supply voltage Nominal operating range: 6 V to 42 V
4	SYNC	Oscillator synchronization input or output The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM25574 devices can be synchronized together by connection of their SYNC pins.
5	COMP	Output of the internal error amplifier The loop compensation network should be connected between this pin and the FB pin.
6	FB	Feedback signal from the regulated output This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225 V.
7	RT	Internal oscillator frequency set input The internal oscillator is set with a single resistor, connected between this pin and the AGND pin.
8	RAMP	Ramp control signal An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50 pF to 2000 pF.
9	AGND	Analog ground Internal reference for the regulator control functions
10	SS	Soft-start An external capacitor and an internal 10 µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, Vcc UVLO and thermal shutdown.
11	OUT	Output voltage connection Connect directly to the regulated output voltage.
12	PGND	Power ground Low side reference for the PRE switch and the IS sense resistor.
13	IS	Current sense Current measurement connection for the re-circulating diode. An internal sense resistor and a sample/hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
14	SW	Switching node The source terminal of the internal buck switch. The SW pin should be connected to the external Schottky diode and to the buck inductor.

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Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
15	PRE	Pre-charge assist for the bootstrap capacitor This open drain output can be connected to SW pin to aid charging the bootstrap capacitor during very light load conditions or in applications where the output may be pre-charged before the LM25574 is enabled. An internal pre-charge MOSFET is turned on for 250 ns each cycle just prior to the on-time interval of the buck switch.
16	BST	Boost input for bootstrap capacitor An external capacitor is required between the BST and the SW pins. A 0.022 µF ceramic capacitor is recommended. The capacitor is charged from Vcc via an internal diode during the off-time of the buck switch.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
V_{IN} to GND		45	V
BST to GND		60	V
PRE to GND		45	V
SW to GND (Steady State)		–1.5	V
BST to V_{CC}		45	V
SD, V_{CC} to GND		14	V
BST to SW		14	V
OUT to GND	Limited	Vin	V
SYNC, SS, FB, RAMP to GND		7	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	6	42	V
T_J Operation junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM25574 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_J = 25°C, and V_{IN} = 24 V, R_T = 32.4 kΩ (unless otherwise noted).[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
VccReg	Vcc Regulator Output	T_J = –40°C to +125°C	6.85	7.15	7.45	V
	Vcc LDO Mode turn-off			9		V
	Vcc Current Limit	Vcc = 0 V		25		mA
VCC SUPPLY						

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are assured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

at T_J = 25°C, and V_{IN} = 24 V, R_T = 32.4 kΩ (unless otherwise noted).[1]

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Vcc UVLO Threshold	(Vcc increasing)	T_J = –40°C to +125°C	5.03	5.35	5.67	V
Vcc Undervoltage Hysteresis				0.35		V
Bias Current (Iin)	FB = 1.3 V	T_J = –40°C to +125°C		3.7	4.5	mA
Shutdown Current (Iin)	SD = 0 V	T_J = –40°C to +125°C		48	70	µA
SHUTDOWN THRESHOLDS						
Shutdown Threshold	(SD Increasing)	T_J = –40°C to +125°C	0.47	0.7	0.9	V
Shutdown Hysteresis				0.1		V
Standby Threshold	(Standby Increasing)	T_J = –40°C to +125°C	1.17	1.225	1.28	V
Standby Hysteresis				0.1		V
SD Pull-up Current Source				5		µA
SWITCH CHARACTERSICS						
Buck Switch Rds(on)	T_J = –40°C to +125°C			750	1500	mΩ
BOOST UVLO				4		V
BOOST UVLO Hysteresis				0.56		V
Pre-charge Switch Rds(on)				70		Ω
Pre-charge Switch on-time				250		ns
CURRENT LIMIT						
Cycle by Cycle Current Limit	RAMP = 0 V	T_J = –40°C to +125°C	0.6	0.7	0.8	A
Cycle by Cycle Current Limit Delay	RAMP = 2.5 V			75		ns
SOFT-START						
SS Current Source	T_J = –40°C to +125°C		7	10	14	µA
OSCILLATOR						
Frequency1	T_J = –40°C to +125°C		180	200	220	kHz
Frequency2	R_T = 11 kΩ	T_J = –40°C to +125°C	425	485	545	kHz
SYNC Source Impedance				11		kΩ
SYNC Sink Impedance				110		Ω
SYNC Threshold (falling)				1.3		V
SYNC Frequency	R_T = 11 kΩ	T_J = –40°C to +125°C	550			kHz
SYNC Pulse Width Minimum	T_J = –40°C to +125°C		15			ns
RAMP GENERATOR						
Ramp Current 1	Vin = 36 V, Vout=10 V	T_J = –40°C to +125°C	272	310	368	µA
Ramp Current 2	Vin = 10 V, Vout=10 V	T_J = –40°C to +125°C	36	50	64	µA
PWM COMPARATOR						
Forced Off-time	T_J = –40°C to +125°C		416	500	575	ns
Min On-time				80		ns
COMP to PWM Comparator Offset				0.7		V

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Electrical Characteristics (continued)

at T_J = 25°C, and V_{IN} = 24 V, R_T = 32.4 kΩ (unless otherwise noted).[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ERROR AMPLIFIER							
	Feedback Voltage	Vfb = COMP	T_J = –40°C to +125°C	1.207	1.225	1.243	V
	FB Bias Current				17		nA
	DC Gain				70		dB
	COMP Sink / Source Current	T_J = –40°C to +125°C		3			mA
	Unity Gain Bandwidth				3		MHz
DIODE SENSE RESISTANCE							
D_{SENSE}					250		mΩ
THERMAL SHUTDOWN							
Tsd	Thermal Shutdown Threshold				165		°C
	Thermal Shutdown Hysteresis				25		°C

6.6 Typical Characteristics

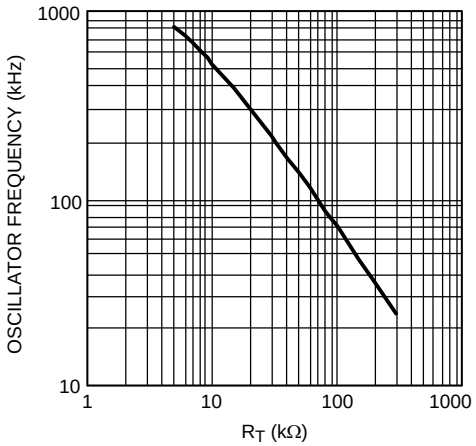

Figure 1. Oscillator Frequency vs R_T

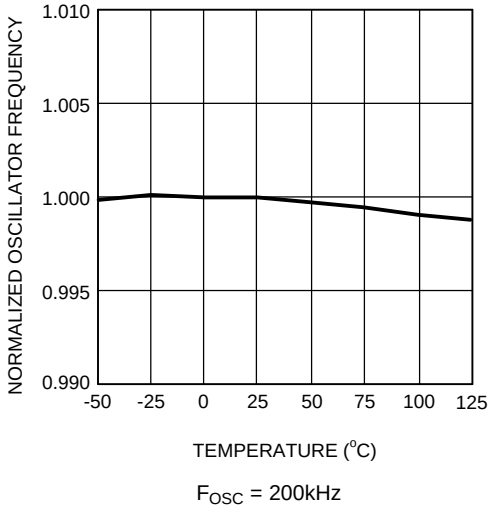

Figure 2. Oscillator Frequency vs Temperature

Typical Characteristics (continued)

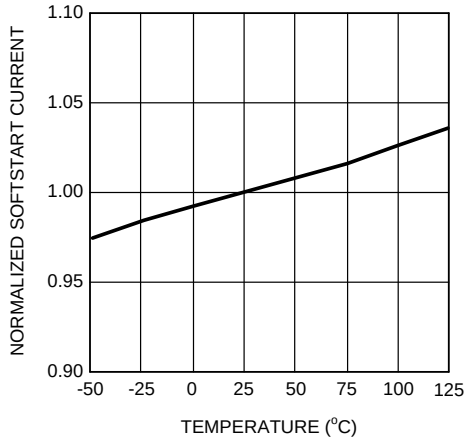

Figure 3. Soft Start Current vs Temperature

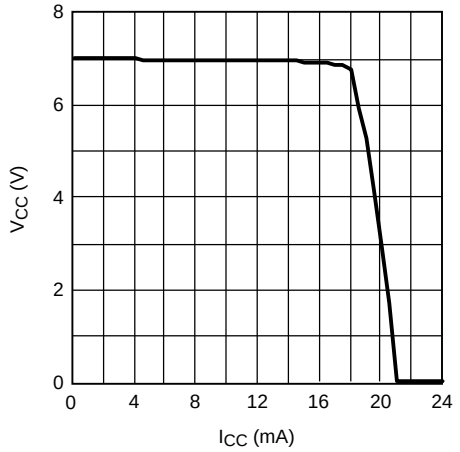

Figure 4. V_{CC} vs I_{CC}

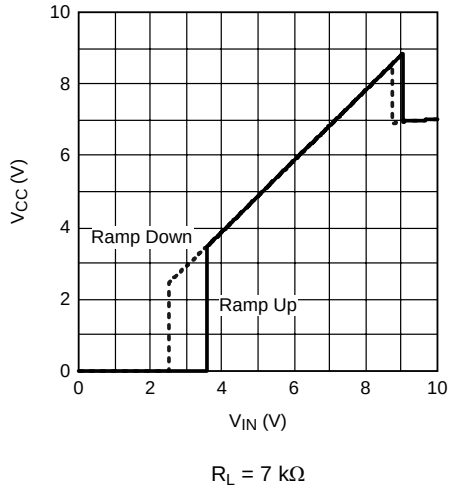

Figure 5. V_{CC} vs V_{IN}

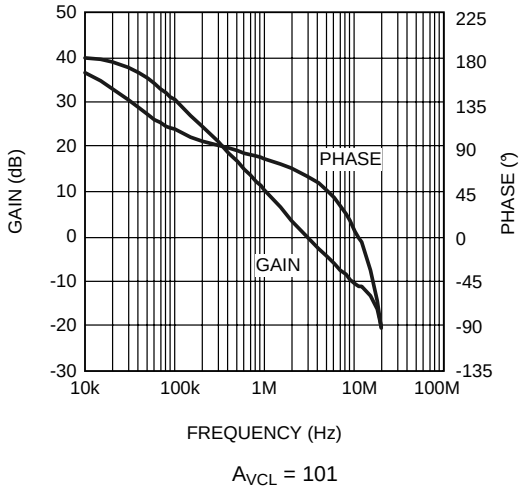

Figure 6. Error Amplifier Gain and Phase

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Typical Characteristics (continued)

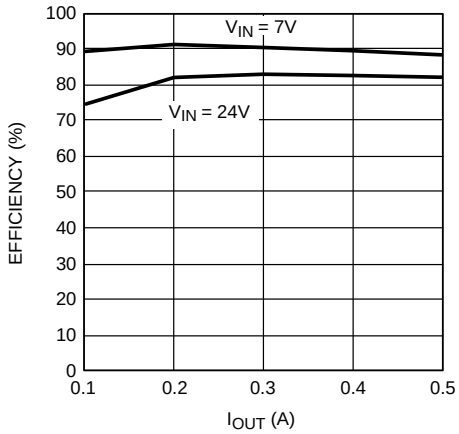


Figure 7. Demoboard Efficiency vs I_{OUT} and V_{IN}

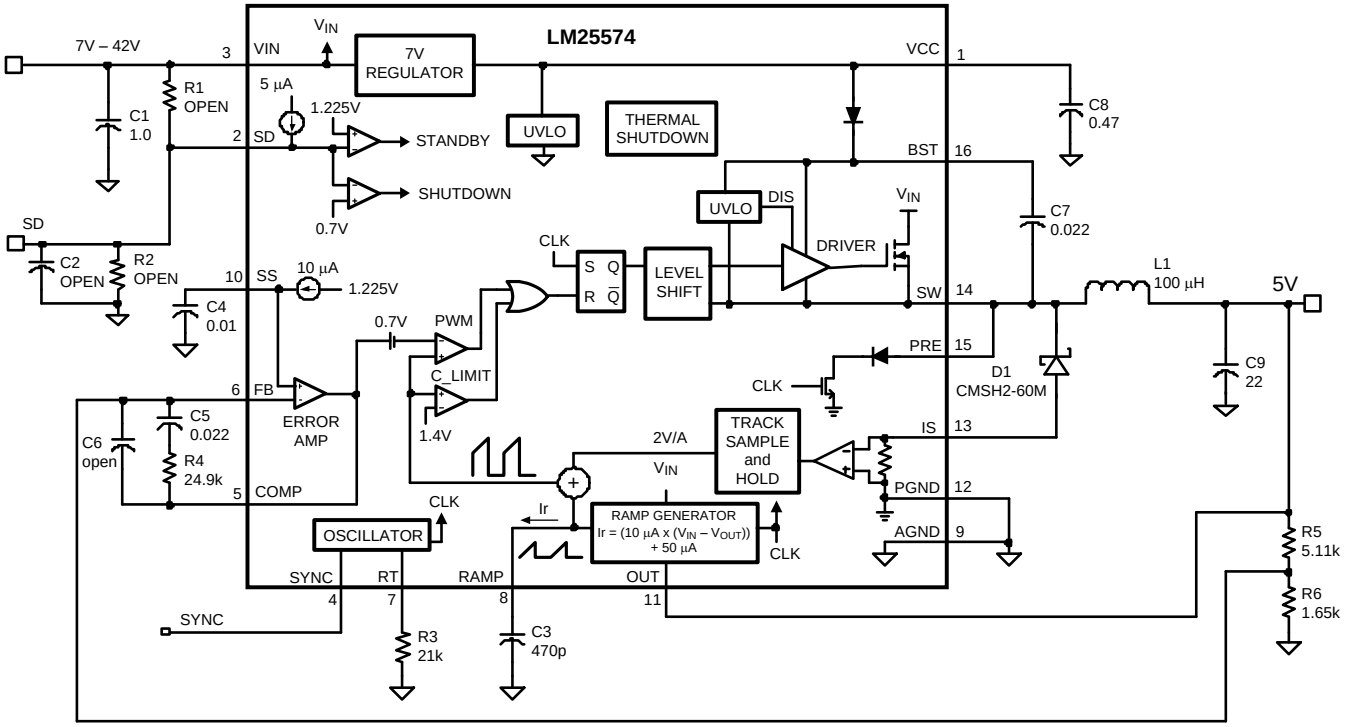
7 Detailed Description

7.1 Overview

The LM25574 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 42-V N-Channel buck switch with an output current capability of 0.5 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 1 MHz. An oscillator synchronization pin allows multiple LM25574 regulators to self synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225 V. Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the TSSOP-16 package.

The functional block diagram and typical application of the LM25574 are shown in *Functional Block Diagram*. The LM25574 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator

The LM25574 contains a dual-mode internal high voltage startup regulator that provides the Vcc bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (VIN) can be connected directly to the input voltage, as high as 42 Volts. For input voltages below 9 V, a low dropout switch connects Vcc directly to Vin. In this supply range, Vcc is approximately equal to Vin. For Vin voltage greater than 9 V, the low dropout switch is disabled and the Vcc regulator is enabled to maintain Vcc at approximately 7 V. The wide operating range of 6 V to 42 V is achieved through the use of this dual mode regulator.

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Feature Description (continued)

The output of the Vcc regulator is current limited to 25 mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the Vcc UVLO threshold of 5.35 V and the SD pin is greater than 1.225 V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until Vcc falls below 5 V or the SD pin falls below 1.125 V.

An auxiliary supply voltage can be applied to the Vcc pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3 V, the internal regulator will essentially shut off, reducing the IC power dissipation. The Vcc regulator series pass transistor includes a diode between Vcc and Vin that should not be forward biased in normal operation. Therefore the auxiliary Vcc voltage should never exceed the Vin voltage.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 45 V. During line or load transients, voltage ringing on the Vin line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

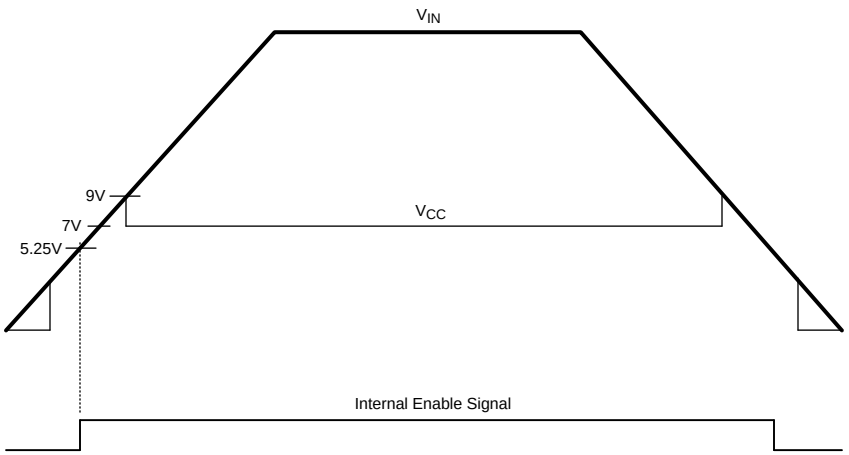

Figure 8. Vin and Vcc Sequencing

7.4 Device Functional Modes

7.4.1 Shutdown and Stand-by Mode

The LM25574 contains a dual level Shutdown (SD) circuit. When the SD pin voltage is below 0.7 V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7 V but less than 1.225 V, the regulator is in standby mode. In standby mode the Vcc regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225 V, the output switch is enabled and normal operation begins. An internal 5 µA pull-up current source configures the regulator to be fully operational if the SD pin is left open.

An external set-point voltage divider from VIN to GND can be used to set the operational input range of the regulator. The divider must be designed such that the voltage at the SD pin will be greater than 1.225 V when Vin is in the desired operating range. The internal 5 µA pull-up current source must be included in calculations of the external set-point divider. Hysteresis of 0.1 V is included for both the shutdown and standby thresholds. The SD pin is internally clamped with a 1 kΩ resistor and an 8 V zener clamp. The voltage at the SD pin should never exceed 14 V. If the voltage at the SD pin exceeds 8 V, the bias current will increase at a rate of 1 mA/V.

The SD pin can also be used to implement various remote enable and disable functions. Pulling the SD pin below the 0.7 V threshold totally disables the controller. If the SD pin voltage is above 1.225 V the regulator will be operational.

7.4.2 Oscillator and Sync Capability

The LM25574 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. The R_T resistor should be located very close to the device and connected directly to the pins of the IC (RT and AGND).To set a desired oscillator frequency (F), the necessary value for the R_T resistor can be calculated Equation 1:

Device Functional Modes (continued)

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

The SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be of higher frequency than the free-running frequency set by the R_T resistor. A clock circuit with an open drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse duration should be greater than 15ns.

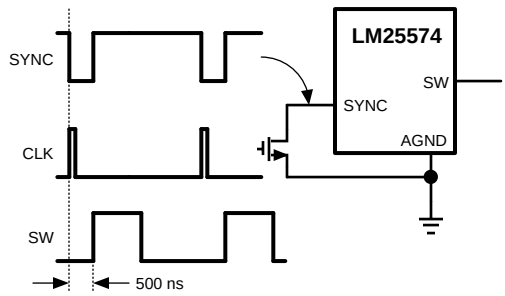

Figure 9. Sync from External Clock

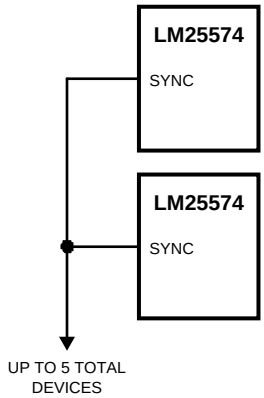

Figure 10. Sync from Multiple Devices

Multiple LM25574 devices can be synchronized together simply by connecting the SYNC pins together. In this configuration all of the devices will be synchronized to the highest frequency device. The diagram in Figure 11 illustrates the SYNC input/output features of the LM25574. The internal oscillator circuit drives the SYNC pin with a strong pull-down and weak pull-up inverter. When the SYNC pin is pulled low either by the internal oscillator or an external clock, the ramp cycle of the oscillator is terminated and a new oscillator cycle begins. Thus, if the SYNC pins of several LM25574 IC's are connected together, the IC with the highest internal clock frequency will pull the connected SYNC pins low first and terminate the oscillator ramp cycles of the other IC's. The LM25574 with the highest programmed clock frequency will serve as the master and control the switching frequency of the all the devices with lower oscillator frequency.

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Device Functional Modes (continued)

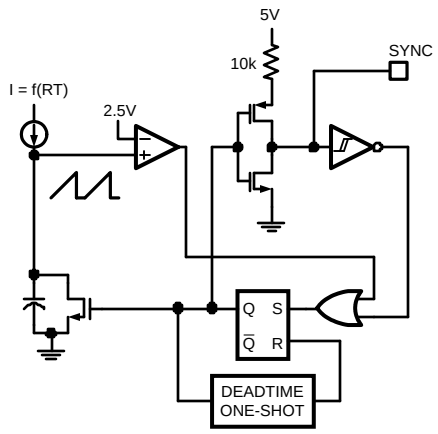

Figure 11. Simplified Oscillator Block Diagram and SYNC I/O Circuit

7.4.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225 V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network, as illustrated in *Functional Block Diagram*. This network creates a pole at DC, a zero and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

7.4.4 Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulsewidth. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulsewidths and duty cycles is necessary for regulation. The LM25574 utilizes a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample and hold DC level and an emulated current ramp.

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Device Functional Modes (continued)

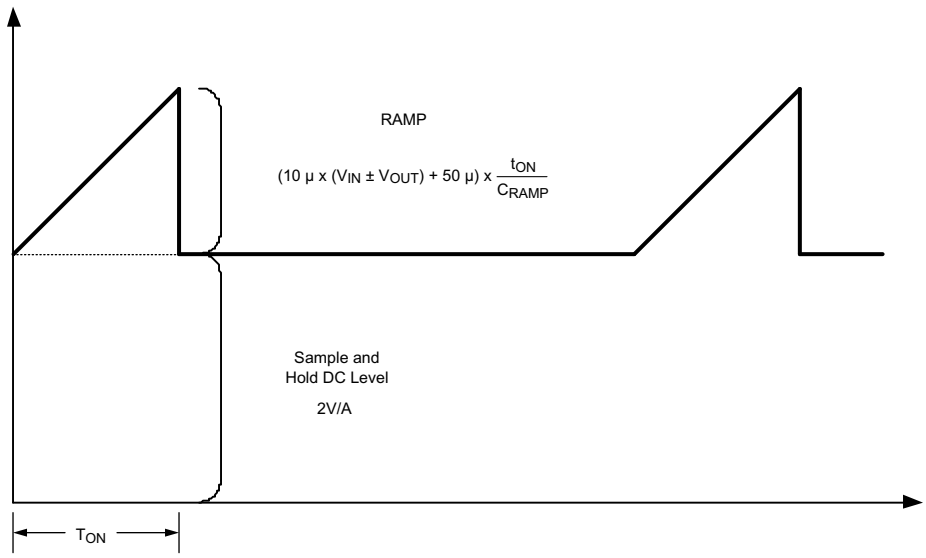

Figure 12. Composition of Current Sense Signal

The sample and hold DC level illustrated in Figure 12 is derived from a measurement of the re-circulating Schottky diode anode current. The re-circulating diode anode should be connected to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample and hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the Vin and Vout voltages per *Equation 2*:

$$I_{RAMP} = (10\mu \times (Vin - Vout)) + 50\mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. The value of C_{RAMP} can be selected from: $C_{RAMP} = L \times 5 \times 10^{-6}$, where L is the value of the output inductor in Henrys. With this value, the scale factor of the emulated current ramp will be approximately equal to the scale factor of the DC level sample and hold (2.0V / A). The C_{RAMP} capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 50 µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, additional slope may be required. In these applications, a pull-up resistor may be added between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5V:

Calculate optimal slope current, $I_{OS} = V_{OUT}$ x 10µA/V.

For example, at V_{OUT} = 10V, I_{OS} = 100µA.

Install a resistor from the RAMP pin to V_{CC}:

$R_{RAMP} = V_{CC} / (I_{OS} - 50\mu A)$

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Device Functional Modes (continued)

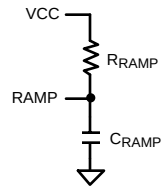

Figure 13. R_{RAMP} to V_{CC} for V_{OUT} > 7.5V

7.4.5 Maximum Duty Cycle and Input Drop-out Voltage

There is a forced off-time of 500 ns implemented each cycle to guarantee sufficient time for the diode current to be sampled. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle will vary with the operating frequency.

$$D_{MAX} = 1 - Fs \times 500\ ns \tag{3}$$

Where Fs is the oscillator frequency. Limiting the maximum duty cycle will raise the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. An approximation of the input dropout voltage is:

$$Vin_{MIN} = \frac{Vout + V_D}{1 - Fs \times 500\ ns} \tag{4}$$

Where V_D is the voltage drop across the re-circulatory diode. Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

7.4.6 Current Limit

The LM25574 contains a unique current monitoring scheme for control and over-current protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 2.0 V / A. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 1.4 V (0.7A) the present current cycle is terminated (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the diode current sampling circuit will detect the excess inductor current during the off-time of the buck switch. If the sample and hold DC level exceeds the 1.4 V current limit threshold, the buck switch will be disabled and skip pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

7.4.7 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10 µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage is connected to the reference input of the error amplifier. Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (over-temperature, Vcc UVLO, SD) the soft-start capacitor will be discharged. When the fault condition is no longer present a new soft-start sequence will commence.

7.4.8 Boost Pin

The LM25574 integrates an N-Channel buck switch and associated floating high voltage level shift / gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022 µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately –0.5 V and the bootstrap capacitor is charged from Vcc through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 500ns to ensure that the bootstrap capacitor is recharged.

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Device Functional Modes (continued)

Under very light load conditions or when the output voltage is pre-charged, the SW voltage will not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor will not receive sufficient voltage to operate the buck switch gate driver. For these applications, the PRE pin can be connected to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 250ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current will flow through the pre-charge MOSFET/diode.

7.4.9 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 External Components

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 1. The circuit shown in *Functional Block Diagram* is configured for the following specifications:

- V_{OUT} = 5 V
- V_{IN} = 7 V to 42 V
- Fs = 300 kHz
- Minimum load current (for CCM) = 100 mA
- Maximum load current = 0.5 A

8.1.2 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 300 kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300 kHz switching frequency can be calculated in Equation 5:

$$R_T = \frac{[(1 / 300 \times 10^3) - 580 \times 10^{-9}]}{135 \times 10^{-12}} \quad (5)$$

The nearest standard value of 21 kΩ was chosen for R_T.

Application Information (continued)

8.1.3 L1

The inductor value is determined based on the operating frequency, load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$).

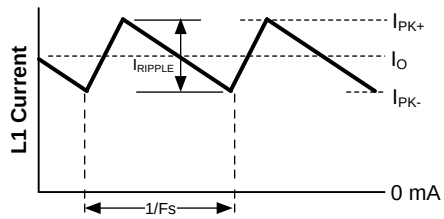

Figure 14. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} should be less than twice the minimum load current, or 0.2 Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \tag{6}$$

$$L1 = \frac{5V \times (42V - 5V)}{0.2A \times 300\ kHz \times 42V} = 73\ \mu H \tag{7}$$

This procedure provides a guide to select the value of L1. The nearest standard value (100µH) will be used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 0.7A nominal (0.85A maximum). The selected inductor (see Table 1) has a conservative 1.0 Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

8.1.4 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is:

$$C_{RAMP} = L \times 5 \times 10^{-6} \tag{8}$$

Where L is in Henrys

With L1 selected for 100µH the recommended value for C3 is 470pF (nearest standard value).

8.1.5 C9

The output capacitor, C9 smoothes the inductor ripple current and provides a source of charge for transient loading conditions. For this design a 22 µF ceramic capacitor was selected. The ceramic capacitor provides ultra low ESR to reduce the output ripple voltage and noise spikes. An approximation for the output ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times F_S \times C_{OUT}}\right) \tag{9}$$

8.1.6 C1

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

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Application Information (continued)

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage effects, one 1.0 µF, 100 V ceramic capacitor will be used. If step input voltage transients are expected near the maximum rating of the LM25574, a careful evaluation of ringing and possible spikes at the device VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

8.1.7 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. A value of 0.47 µF was selected for this design.

8.1.8 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022 µF, and should be a good quality, low ESR, ceramic capacitor.

8.1.9 C4

The capacitor at the SS pin determines the soft-start time, that is the time for the reference voltage and the output voltage, to reach the final regulated value. The time is determined from Equation 10:

$$t_{ss} = \frac{C4 \times 1.225V}{10\ \mu A} \tag{10}$$

For this application, a C4 value of 0.01µF was chosen which corresponds to a soft-start time of 1ms.

8.1.10 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated from Equation 11:

$$R5/R6 = (V_{OUT} / 1.225V) - 1 \tag{11}$$

For a 5 V output, the R5 and R6 ratio calculates to 3.082. The resistors should be chosen from standard value resistors, a good starting point is selection in the range of 1.0 kΩ - 10 kΩ. Values of 5.11 kΩ for R5, and 1.65 kΩ for R6 were selected.

8.1.11 R1, R2, C2

A voltage divider can be connected to the SD pin to set a minimum operating voltage $Vin_{(min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (between 10 kΩ and 100 kΩ recommended) then calculate R2 from Equation 12:

$$R2 = 1.225 \times \left(\frac{R1}{V_{IN(min)} + (5 \times 10^{-6} \times R1) - 1.225}\right) \tag{12}$$

Capacitor C2 provides filtering for the divider. The voltage at the SD pin should never exceed 8 V, when using an external set-point divider it may be necessary to clamp the SD pin at high input voltage conditions. The reference design utilizes the full range of the LM25574 (6 V to 42 V); therefore these components can be omitted. With the SD pin open circuit the LM25574 responds once the Vcc UVLO threshold is satisfied.

8.1.12 R4, C5, C6

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM25574 is as follows:

$$DC\ Gain_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 0.5 \times R_{LOAD} \tag{13}$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD},) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{p(MOD)} = 1 / (2\pi\ R_{LOAD}\ C_{OUT}) \tag{14}$$

Application Information (continued)

For R_{LOAD} = 20Ω and C_{OUT} = 22µF then $f_{p(MOD)}$ = 362Hz

DC $Gain_{(MOD)}$ = 0.5 x 20 = 20dB

For the design example of *Functional Block Diagram* the following modulator gain vs. frequency characteristic was measured as shown in Figure 15.

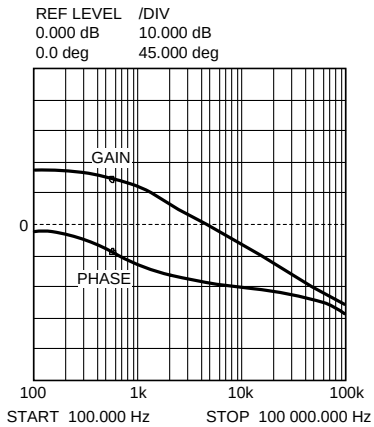

Figure 15. Gain and Phase of Modulator R_{LOAD} = 20 Ohms and C_{OUT} = 22µF

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 / (2πR4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 25kHz was selected. The compensation network zero (f_Z) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 / (2π R4 C5) to be less than 2 kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example C5 was selected for 0.022 µF and R4 was selected for 24.9 kΩ. These values configure the compensation network zero at 290 Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 5 (14dB).

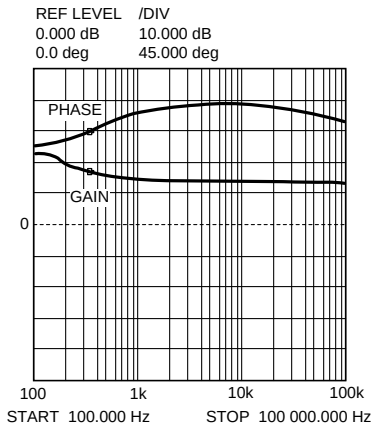

Figure 16. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

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Application Information (continued)

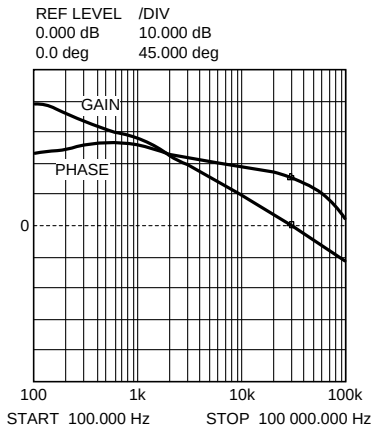

Figure 17. Overall Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C6 can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C6 must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is: f_{p2} = fz x C5 / C6.

8.1.13 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step-down the input voltage V_{IN} to a nominal V_{CC} level of 7V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the Vcc regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 18 and Figure 19 depict two methods to bias the IC from the output voltage. In each case the internal Vcc regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7 V regulation level, which effectively disables the internal V_{CC} regulator. The voltage applied to the VCC pin should never exceed 14 V. The V_{CC} voltage should never be larger than the V_{IN} voltage.

Application Information (continued)

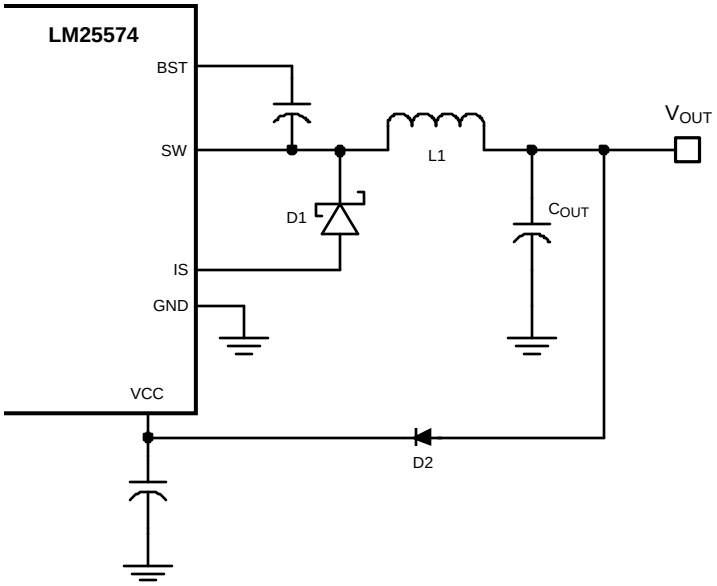

Figure 18. VCC Bias from VOUT for 8V < VOUT < 14V

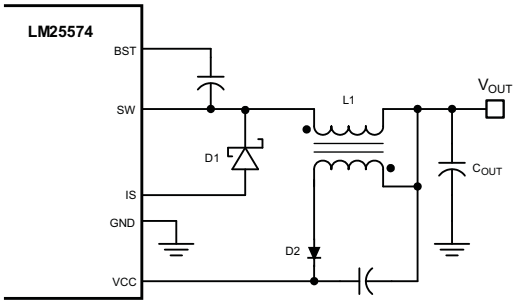

Figure 19. VCC Bias with Additional Winding on the Output Inductor

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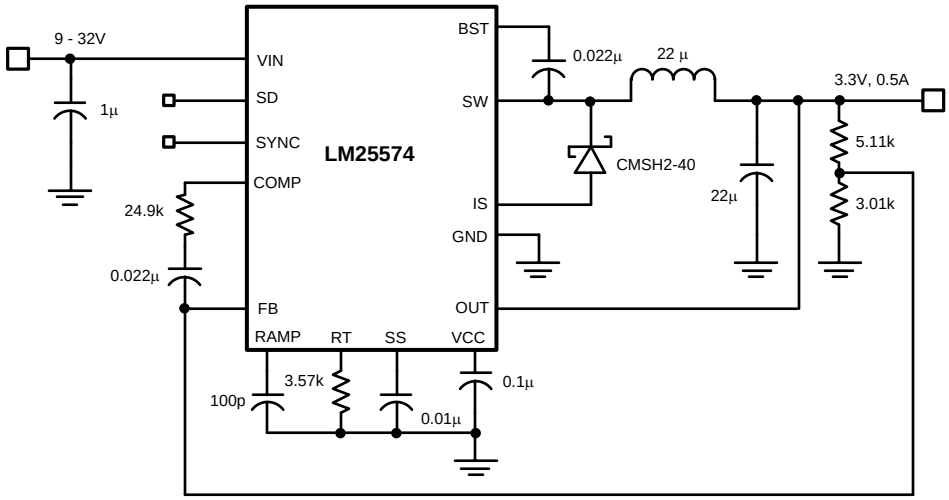
8.2 Typical Application

8.2.1 Typical Schematic for High Frequency (1MHz) Application



8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25574 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9 Layout

9.1 Layout Guidelines

9.1.1 PCB Layout and Thermal Considerations

The circuit in *Functional Block Diagram* serves as both a block diagram of the LM25574 and a typical application board schematic for the LM25574. In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper trace. Place several vias in this trace to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM25574 regulator IC. The easiest method to determine the power dissipated within the LM25574 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. An approximation for the Schottky diode loss is P = (1-D) x Iout x Vfwd. An approximation for the output inductor power is $P = I_{OUT}^2 \times R \times 1.1$, where R is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses. If a snubber is used, an approximation for the damping resistor power dissipation is $P = Vin^2 \times Fsw \times Csnub$, where Fsw is the switching frequency and Csnub is the snubber capacitor.

The most significant variables that affect the power dissipated by the LM25574 are the output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input volatge can be appreciable. The operating frequency of the LM25574 evaluation board has been designed for 300 kHz. When operating at 0.5 A output current with a 42 V input the power dissipation of the LM25574 regulator is approximately 0.36 W.

The junction-to-ambient thermal resistance of the LM25574 will vary with the application. The most significant variables are the area of copper in the PC board, and the amount of forced air cooling provided. The junction-to-ambient thermal resistance of the LM25574 mounted in the evaluation board varies from 90°C/W with no airflow to 60°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM25574 will be 25 + (90 x 0.36) = 57°C. If the evaluation board is operated at 0.5 A output current, 42 V input voltage and high ambient temperature for a prolonged period of time the thermal shutdown protection within the IC may activate. The IC will turn off allowing the junction to cool, followed by restart with the soft-start capacitor reset to zero.

Table 1. 5V, 0.5A Demo Board Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C3225X7R2A105M	CAPACITOR, CER, TDK	1µ, 100V
C	2	OPEN	NOT USED	
C	3	C0805A471K1GAC	CAPACITOR, CER, KEMET	470p, 100V
C	4	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01µ, 100V
C	5	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022µ, 100V
C	6	OPEN	NOT USED	
C	7	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022µ, 100V
C	8	C2012X7R1C474M	CAPACITOR, CER, TDK	0.47µ, 16V
C	9	C3225X7R1C226M	CAPACITOR, CER, TDK	22µ, 16V
D	1	CMSH2-60M	DIODE, 60V, CENTRAL	
L	1	DR74-101	INDUCTOR, COOPER	100µH
R	1	OPEN	NOT USED	
R	2	OPEN	NOT USED	
R	3	CRCW08052102F	RESISTOR	21kΩ
R	4	CRCW08052492F	RESISTOR	24.9kΩ

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Layout Guidelines (continued)

Table 1. 5V, 0.5A Demo Board Bill of Materials (continued)

ITEM		PART NUMBER	DESCRIPTION	VALUE
R	5	CRCW08055111F	RESISTOR	5.11kΩ
R	6	CRCW08051651F	RESISTOR	1.65kΩ
U	1	LM25574	REGULATOR, TEXAS INSTRUMENTS	

9.2 Layout Example

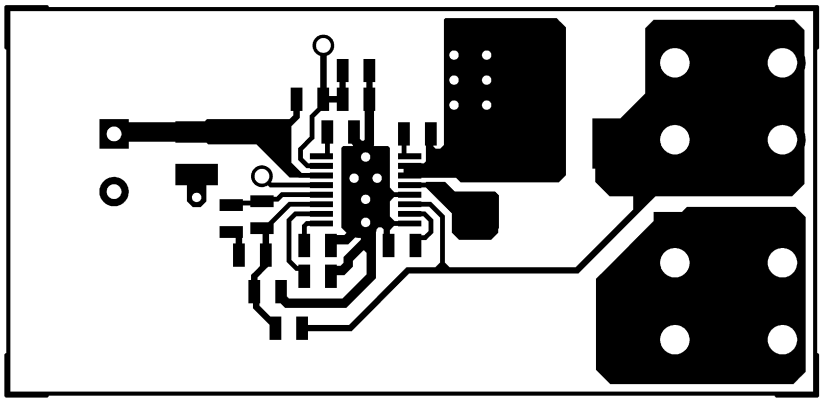

Figure 20. Component Side

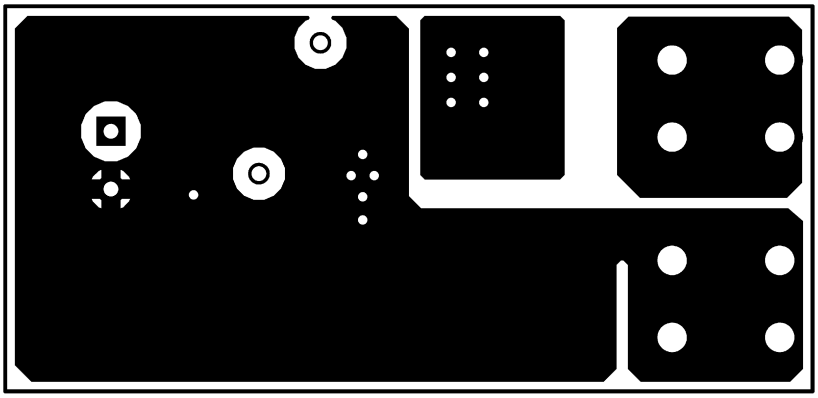

Figure 21. Solder Side

Layout Example (continued)

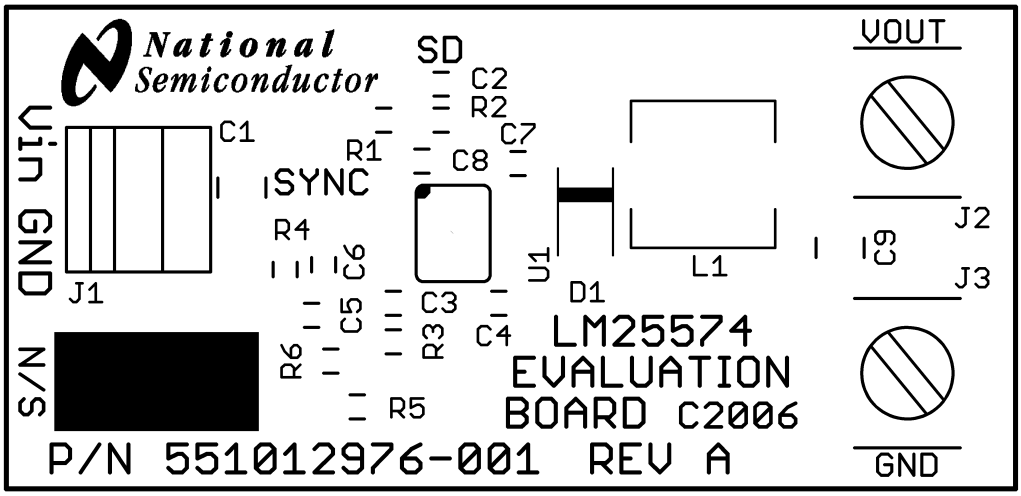

Figure 22. Silkscreen

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Developmental Support

10.1.1.1 Custom Design With WEBENCH® Tools

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1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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3. Compare the generated design with other possible solutions from Texas Instruments.

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- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25574MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L25574 MT	Samples
LM25574MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L25574 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM25574 :

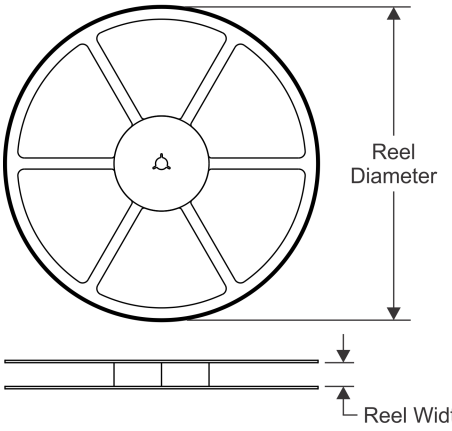
- Automotive: LM25574-Q1

NOTE: Qualified Version Definitions:

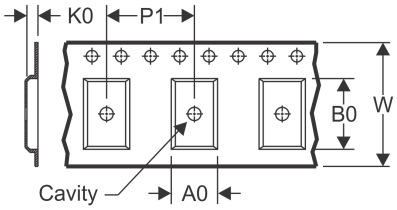
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

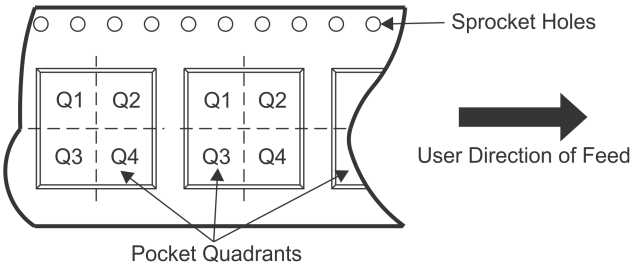


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

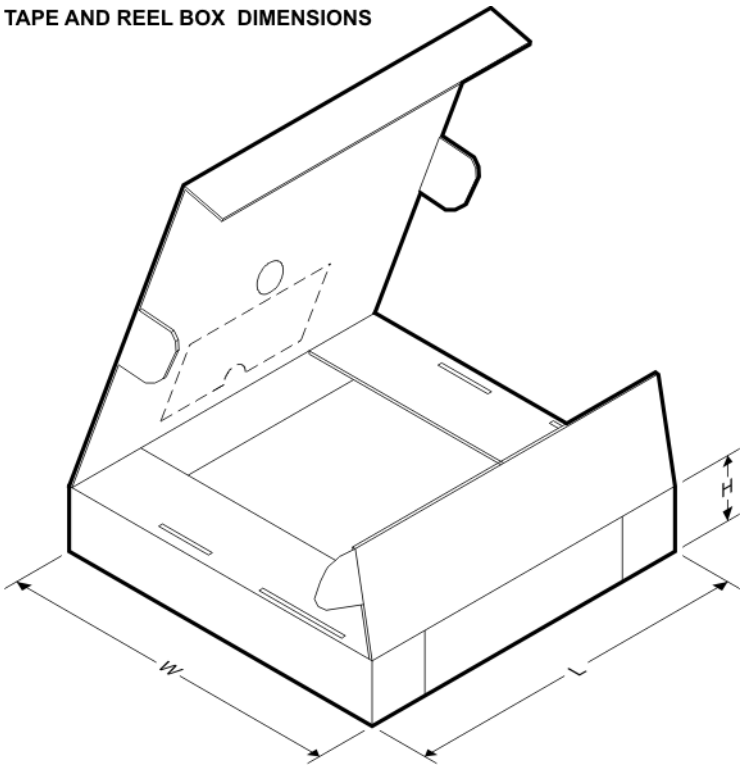
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25574MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

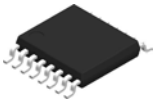
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25574MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

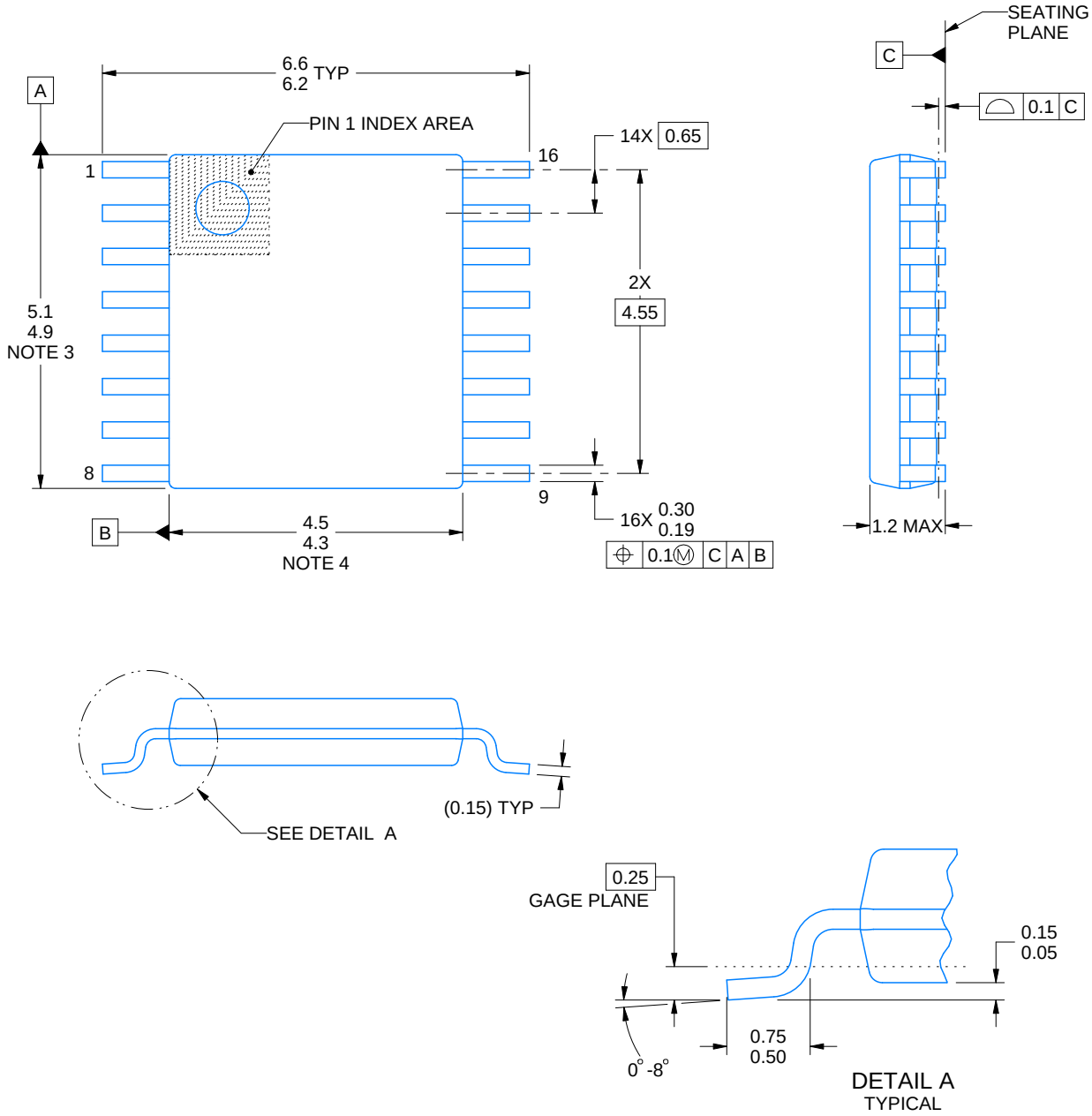
PW0016A



PACKAGE OUTLINE

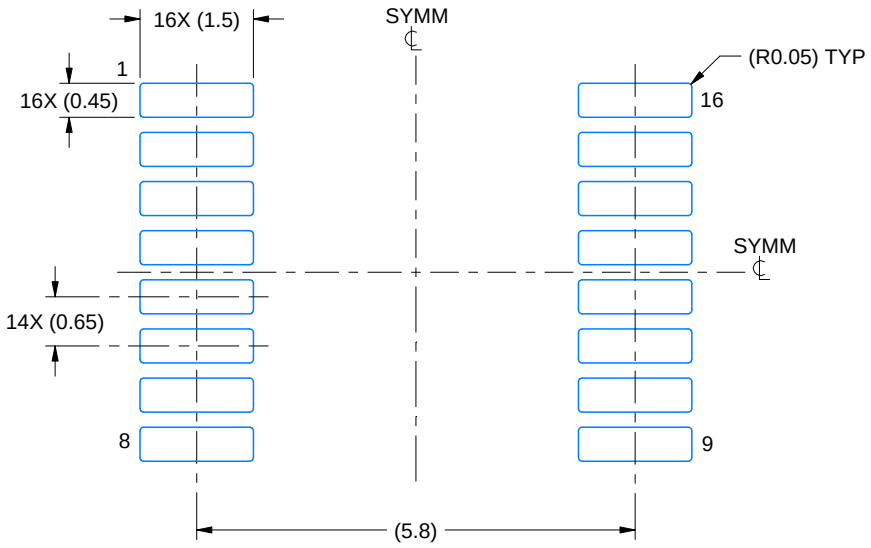
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

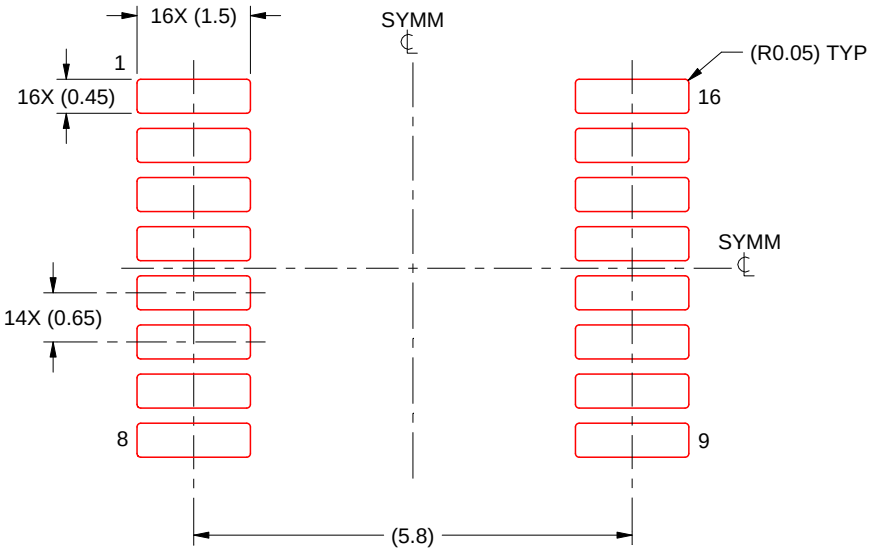
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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